CLAIMS

What is claimed is:

1. A method of providing an optimal memory access strobe, comprising:

determining an initial delay for a data access signal to a memory device by employing a delay locked loop (DLL) circuit to delay said data access signal to a center of a data window;

performing a memory test of said memory device; and

adjusting said initial delay by a fine tuning offset determined by said memory test.

2. The method of providing an optimal memory access strobe according to claim 1, wherein:

said data access signal is a DQS strobe.

3. The method of providing an optimal memory access strobe according to claim 1, wherein:

said data access signal is a read data access clock signal.

4. The method of providing an optimal memory access strobe according to claim 1, wherein:

said data access signal is a write data access clock signal.

5. The method of providing an optimal memory access strobe according to claim 4, wherein:

said DQS strobe relates to a DDR-RAM device.

6. The method of providing an optimal memory access strobe according to claim 5, wherein:

said DQS strobe relates to a DDR-SDRAM device.

7. The method of providing an optimal memory access strobe according to claim 1, wherein:

said data window is a read data window.

8. The method of providing an optimal memory access strobe according to claim 1, wherein:

said data window is a write data window.

9. The method of providing an optimal memory access strobe according to claim 1, further comprising:

further adjusting said initial delay in correlation to actual environmental conditions using a PVT circuit.

10. Apparatus for providing an optimal memory access strobe, comprising:

means for determining an initial delay for a data access signal to a memory device by employing a delay locked loop (DLL) circuit to delay said data access signal to a center of a data window;

means for performing a memory test of said memory device; and

means for adjusting said initial delay by a fine tuning offset determined by said memory test.

11. The apparatus for providing an optimal memory access strobe according to claim 10, wherein:

said data access signal is a DQS strobe.

12. The apparatus for providing an optimal memory access strobe according to claim 10, wherein:

said data access signal is a read data access clock signal.

13. The apparatus for providing an optimal memory access strobe according to claim 10, wherein:

said data access signal is a write data access clock signal.

14. The apparatus for providing an optimal memory access strobe according to claim 13, wherein:

said DQS strobe relates to a DDR-RAM device.

15. The apparatus for providing an optimal memory access strobe according to claim 14, wherein:

said DQS strobe relates to a DDR-SDRAM device.

16. The apparatus for providing an optimal memory access strobe according to claim 10, wherein:

said data window is a read data window.

17. The apparatus for providing an optimal memory access strobe according to claim 10, wherein:

said data window is a write data window.

18. The apparatus for providing an optimal memory access strobe according to claim 10, further comprising:

PVT adjustment circuit means for further adjusting said initial delay in correlation to actual environmental conditions.

19. A DQS strobe controller for a double data rate (DDR) memory device, comprising:

a delay line formed by a plurality of programmable delay elements to provide an initial delay; and

an adder/subtracter element for implementing a fine tuning adjustment of said initial delay, said fine tuning adjustment being determined empirically by operation of said DQS strobe controller in operation with said DDR memory device.

20. The DQS strobe controller for a double data rate (DDR) memory device according to claim 19, further comprising:

a PVT circuit to provide an additional fine tuning adjustment of said initial delay.

21. The DQS strobe controller for a double data rate (DDR) memory device according to claim 19, wherein:

said fine tuning adjustment is determined empirically by way of a memory test of said actual DDR memory device.